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NTE7206
Integrated Circuit
Triple Video Output Amplifier

Description:

The NTE7206 includes three video output amplifiers in one plastic 9–Lead SIP medium power package, using high–voltage DMOS technology, and is intended to drive the three cathodes of a color CRT directly. To obtain maximum performance, the amplifier should be used with black–current control.

Features:

- Typical Bandwidth of 5.5MHz for an Output Signal of 60V (p–p)
- High Slew Rate of 900V/μs
- No External Components Required
- Very Simple Application
- Single Supply Voltage of 200V
- Internal Reference Voltage of 2.5V
- Fixed Gain of 50
- Black–Current Stabilization (BCS) Circuit
- Thermal Protection.

Absolute Maximum Ratings: (Voltages measured with respect to Pin4 (GND) unless otherwise specified)

Supply Voltage, V_{DD} 250V
Input Voltage at Pin1 to Pin3, V_i 12V
Measurement Output Voltage, $V_{o(m)}$ 6V
Cathode Output Voltage, $V_{o(c)}$ . . . . . V_{DD}
Junction Temperature Range, T_j . . . . . –20° to +150°C
Storage Temperature Range, T_{stg} . . . . . –55° to +150°C
Electrostatic Handling, V_{es}
Human Body Model (HBM) 2000V
Machine Model (MM) 300V
Thermal Resistance, Junction–to–Ambient, $R_{th(JA)}$ 56K/W
Thermal Resistance, Junction–to–Fin (Note 1), $R_{th(J-FIN)}$ 11K/W
Thermal Resistance, Heatsink–to–Ambient, $R_{th(H-A)}$ 18K/W

Note 1. An external heatsink is necessary.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		180	–	210	V
Operating Range	T_j		–20	–	+150	°C

Electrical Characteristics: (T_A = +25°C, V_{DD} = 200V, $V_{o(c1)} = V_{o(c2)} = V_{o(c3)} = 1/2V_{DD}$, C_L = 10 pF (C_L consists of parasitic and cathode capacitance), $R_{th(H-A)}$ = 18K/W unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Supply Current	I_q		5.9	6.9	7.9	mA
Internal Reference Voltage (input stage)	$V_{ref(int)}$			2.5		V
Input Resistance	R_i			3.6		kΩ
Gain of Amplifier	G		47.5	51.0	55.0	
Gain Difference	ΔG		−2.5	0	+2.5	
Nominal Ouput Voltage at Pin7, Pin8 and Pin9 (DC Value)	$V_{O(c)}$	I_i = 0μA	116	129	142	V
Differential Nominal Output Offset Voltage between Pin7 and Pin8, Pin8 and Pin9 and Pin9 and Pin7 (DC Value)	$\Delta V_{O(c)(offset)}$	I_i = 0μA		0	5	V
Output Voltage Temperature Drift at Pin7, Pin8 and Pin9	$\Delta V_{O(c)(T)}$			−10		mV/K
Differential Output Offset Temperature Drift between Pin7 and Pin8, Pin8 and Pin9 and Pin7 and Pin9	$\Delta V_{O(c)(T)(offset)}$			0		mV/K
Offset Current of Measurement Output	$I_{o(m)(offset)}$	$I_{o(c)}$ = 0μA, 1.5V < V_i < 5.5V, 3V < $V_{o(m)}$ < 6V	−50		+50	μA
Linearity of Current Transfer	$\Delta I_{o(m)}/\Delta I_{o(c)}$	−100μA < $I_{o(c)}$ < 100μA, 1.5V < V_i < 5.5V, 3V < $V_{o(m)}$ < 6V	0.9	1.0	1.1	
		at CRT discharge, $I_{o(c)}$ = 1mA, 1.5V < V_i < 5.5V, 3V < $V_{o(m)}$ < 5.4V		1.0		
Maximum Peak Output Current (Pin7, Pin8 and Pin9)	$I_{o(c)(max)}$	50V < $V_{o(c)}$ < V_{DD} − 50V		20		mA
Minimum Output Voltage (Pin7, Pin8 and Pin9)	$V_{o(c)(min)}$	V = 7V			10	V
Maximum Output Voltage (Pin7, Pin8 and Pin9)	$V_{o(c)(max)}$	V = 1V	V_{DD}−15			V
Small Signal Bandwidth (Pin7, Pin8 and Pin9)	B_S	$V_{o(c)}$ = 60V(p−p)		5.5		MHz
Large Signal Bandwidth (Pin7, Pin8 and Pin9)	B_L	$V_{o(c)}$ = 100V(p−p)		4.5		MHz
Cathode Output Propagation Time 50% input to 50% output (Pin7, Pin8 and Pin9)	t_{Pco}	$V_{o(c)}$ = 100V(p−p) square wave, f < 1MHz, t_r = t_f = 40ns (Pin1, Pin2 and Pin3)		60		ns
Difference in Cathode Output Propagation Time 50% input to 50% output (Pin7 and Pin8, Pin7 and Pin9 and Pin8 and Pin9)	Δt_{Pco}	$V_{o(c)}$ = 100V(p−p) square wave, f < 1MHz, t_r = t_f = 40ns (Pin1, Pin2 and Pin3)	−10	0	+10	ns
Cathode Output Rise Time 10% Output to 90% Output (Pin7, Pin8 and Pin9)	$t_{o(r)}$	$V_{o(c)}$ = 50 to 150V square wave, f < 1MHz; t_f = 40ns (Pin1, Pin2 and Pin3)	67	91	113	ns
Cathode Output Fall Time 90% output to 10% Output (Pin7, Pin8 and Pin9)	$t_{o(f)}$	$V_{o(c)}$ = 150 to 50V square wave, f < 1MHz, t_r = 40ns (Pin1, Pin2 and Pin3)	67	91	113	ns

Electrical Characteristics (Cont'd): (T_A = +25°C, V_{DD} = 200V, $V_{o(c1)}$ = $V_{o(c2)}$ = $V_{o(c3)}$ = 1/2V_{DD}, C_L = 10 pF (C_L consists of parasitic and cathode capacitance), $R_{th(H-A)}$ = 18K/W unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setting Time 50% Input to 99% < output < 101% (Pin7, Pin8 and Pin9)	t_{st}	$V_{o(c)}$ = 100V(p-p) square wave, f < 1MHz; t_r = t_f = 40ns (Pin1, Pin2 and Pin3)			350	ns
Slew Rate Between 50V to (V_{DD} - 50V) (Pin7, Pin8 and Pin9)	SR	V_i = 4V (p-p) square wave, f < 1MHz; t_r = t_f = 40ns (Pin1, Pin2 and Pin3)		900		V/µs
Cathode Ouput Voltage Overshoot (Pin7, Pin8 and Pin9)	O_v	$V_{o(c)}$ = 100V (p-p) square wave, f < 1MHz; t_r = t_f = 40ns (Pin1, Pin2 and Pin3)		2		%
Power Supply Rejection Ratio	PSRR	f < 50kHz, Note 2		55		dB
DC Crosstalk Between Channels	$\alpha_{ct(DC)}$			50		dB

Note 2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Pin Connection Diagram
(Front View)