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NTE40107B
Integrated Circuit
CMOS – Dual 2 Input NAND Buffer/Driver

Description:

The NTE40107B is a dual, 2–input, NAND buffer/driver in an 8–Lead DIP type package containing two independent 2–input NAND buffers with open–drain single N–Channel transistor outputs. This device features a wired–OR capability and high output sink current capability (136mA Typ. at V_{DD} = 10V, V_{DS} = 1V).

Features:

- 32 Times Standard B–Series Output Current Drive Sinking Capability:
  136mA Typ. at V_{DD} = 10V, V_{DS} = 1V
- 100% Tested for Quescient Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- 5V, 10V, and 15V Parametric Ratings
- Noise margin, Full Package Temperature Range, R_L to V_{DD} = 10kΩ:
  1V at V_{DD} = 5V
  2V at V_{DD} = 10V
  2.5V at V_{DD} = 15V

Applications:

- Driving Relays, Lamps, and LEDs
- Line Driver
- Level Shifter (Up of Down)

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages Referenced to V_{SS} Terminal), V_{DD} . . . . . –0.5V to +2.0V
Input Voltage Range, All Inputs . . . . . –0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Power Dissipation Per Package, P_D
For T_A = –55° to +100°C 500mW
For T_A = +100° to +125°C . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation Per Output Transistor (T_A = Full Package Temperature Range) 100mW
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 1/16” from Case for 10sec Max), T_L . . . . . +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}	T_A = –55° to +125°C	3	–	18	V

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Dynamic Electrical Characteristics: (T_A = +25°C, C_L = 50pF, Input t_r, t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay, High−to−Low	t_{PHL}	R_L = 120Ω, Note 2	V_{DD} = 5V	−	100	200	ns
			V_{DD} = 10V	−	45	90	ns
			V_{DD} = 15V	−	30	60	ns
Propagation Delay, Low−to−High	t_{PLH}	R_L = 120Ω, Note 2	V_{DD} = 5V	−	100	200	ns
			V_{DD} = 10V	−	60	120	ns
			V_{DD} = 15V	−	50	100	ns
Transition Time, High−to−Low	t_{THL}	R_L = 120Ω, Note 2	V_{DD} = 5V	−	50	100	ns
			V_{DD} = 10V	−	20	40	ns
			V_{DD} = 15V	−	10	20	ns
Transition Time, Low−to−High	t_{TLH}	R_L = 120Ω, Note 2	V_{DD} = 5V	−	50	100	ns
			V_{DD} = 10V	−	35	70	ns
			V_{DD} = 15V	−	25	50	ns
Average Input Capacitance	C_{IN}	Any Input		−	5.0	7.5	pF
Average Output Capacitance	C_{OUT}	Any Output		−	30	−	pF

Note 2. R_L is external pull−up resistor to V_{DD}.

Static Electrical Characteristics:

Parameter	Symbol	Conditions			Limits at Indicated Temperatures (°C)							Unit
									+25			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min	Typ	Max	
Quiescent Device Current	I_{DD}Max	−	0.5	5	1	1	30	30	−	0.02	1	μA
		−	0,10	10	2	2	60	60	−	0.02	2	μA
		−	0,15	15	4	4	120	120	−	0.02	4	μA
		−	0,20	20	20	20	600	600	−	0.04	20	μA
Output Low (Sink) Current	I_{OL}Min	0.4	0,5	5	21	20	14	12	16	32	−	mA
		1	0,5	5	44	42	30	25	34	68	−	mA
		0.5	0,10	10	49	46	32	28	37	74	−	mA
		1	0,10	10	89	85	60	51	68	136	−	mA
		0.5	0,15	15	66	63	44	38	50	100	−	mA
Output High (Source) Current	I_{OH}Min	No Internal Pull−Up Devices										mA
Input Low Voltage (Note 3)	V_{IL}Max	4.5	−	5	−	1.5			−	−	1.5	V
		9	−	10	−	3.0			−	−	3.0	V
		13.5	−	15	−	4.0			−	−	4.0	V
Input High Voltage (Note 3)	V_{IH}Min	0.5,4.5	−	5	−	3.5			3.5	−	−	V
		1,9	−	10	−	7			7	−	−	V
		1.5,13.5	−	15	−	11			11	−	−	V
Input Current	I_{IN}Max	−	0,18	18	±0.1	±0.1	±1	±1	−	$\pm10^{-5}$	±0.1	μA
Output Leakage Current	I_{OZ}Max	18	0,18	18	2	2	20	20	−	10^{-4}	2	μA

Note 3. Measured with external pull−up resistor, R_L = 10kΩ to V_{DD}.

Special Considerations:

Limiting Capacitive Currents for C_L > 500pF, V_{DD} > 15V. For V_{DD} > 15V, and load capacitance (C_L) from output to GND > 500pF, an external 25Ω series limiting resistor should be inserted between the output terminal and C_L. No external resistor is necessary if C_L < 500pF of V_{DD} < 15V.

Driving Inductive Loads. When using the NTE40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the device output.

Truth Table:

A	B	C	
0	0	1 *	Z #
1	0	1 *	Z #
0	1	1 *	Z #
1	1	0	

* Requires external pull−up resistor (R_L) to V_{DD}.

\# Without pull−up resistor (3−state).

Pin Connection Diagram
(Top View)